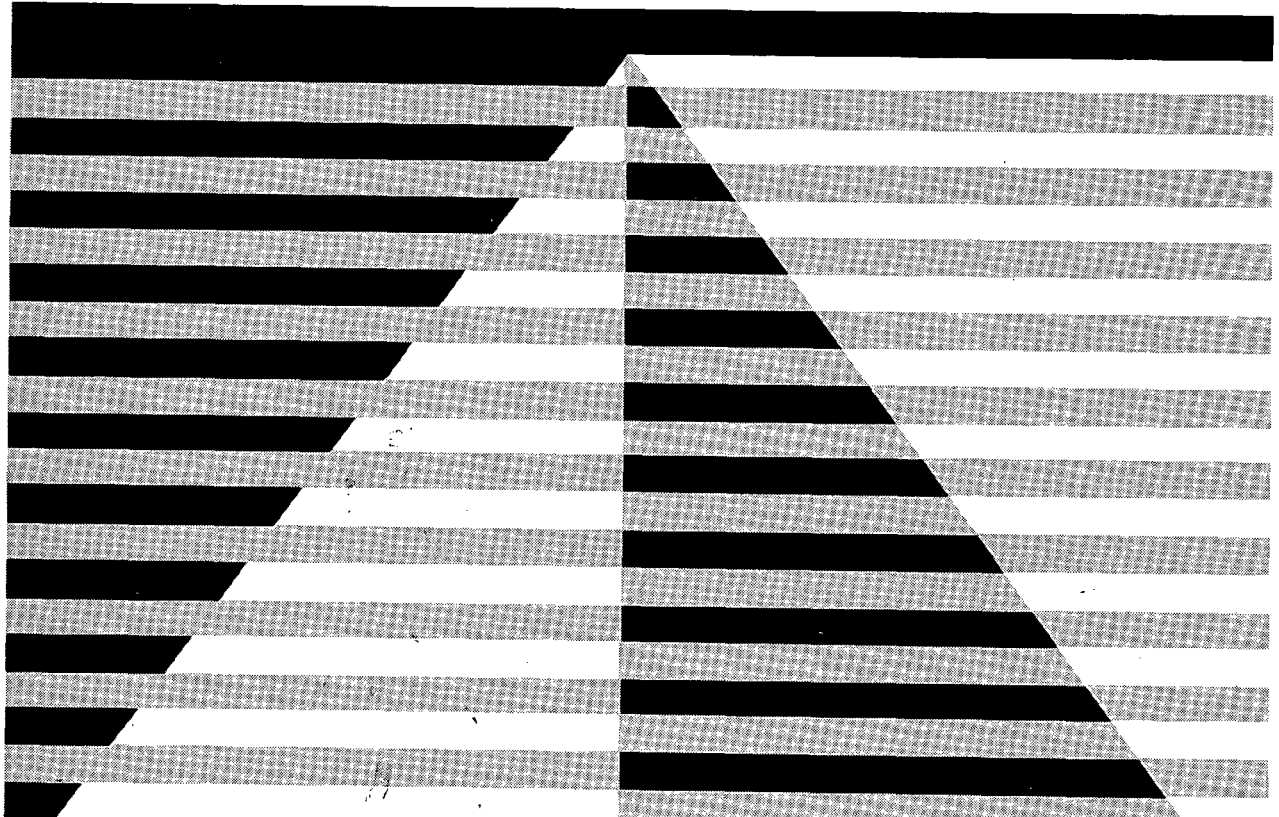


COMPUTER ARCHITECTURE NEWS  
Volume 15, Number 2  
June 1987




June 2-5, 1987  
Pittsburgh, Pennsylvania

The 14th Annual  
International Symposium on

# COMPUTER ARCHITECTURE



**SPONSORED BY**

-  IEEE COMPUTER SOCIETY  
Technical Committee on Computer Architecture
-  Association for Computing Machinery  
SIGARCH
-  THE INSTITUTE OF ELECTRICAL  
AND ELECTRONICS ENGINEERS, INC.

## CONFERENCE PROCEEDINGS

IEEE COMPUTER SOCIETY ORDER NUMBER 776  
LIBRARY OF CONGRESS NUMBER 85-642869  
IEEE CATALOG NUMBER 87CH2420-6  
ISBN 0-8188-0776-8  
ISSN 0884-7495  
ACM ORDER NUMBER 415870  
ISBN 0-89791-233-0

Technische Hochschule Darmstadt  
FACHBEREICH INFORMATIK

BIBLIOTHEK

Inventar-Nr.: 6303

Sachgebiete: \_\_\_\_\_

Standort: \_\_\_\_\_

Fachbereichsbibliothek Informatik  
TU Darmstadt



 THE COMPUTER SOCIETY  
OF THE IEEE



IEEE

THE INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS, INC.

COMPUTER  
SOCIETY  
PRESS 

# Table of Contents

<b>Message from General Chairman</b> .....	iii
<b>Program Chairman's Remarks</b> .....	v
<b>General Conference Committee</b> .....	vi
<b>Program Committee</b> .....	vii
 <b>Branching Techniques</b>	
Branch Folding in the CRISP Microprocessor: Reducing Branch Delay to Zero .....	2
<i>D.R. Ditzel and H.R. McLellan</i>	
An Evaluation of Branch Architectures .....	10
<i>J.A. DeRosa and H.M. Levy</i>	
 <b>Pipelining</b>	
Checkpoint Repair for Out-of-Order Execution Machines .....	18
<i>W.W. Hwu and Y.N. Patt</i>	
Instruction Issue Logic for High-Performance, Interruptable Pipelined Processors .....	27
<i>G.S. Sohi and S. Vajapeyam</i>	
Fast Temporary Storage for Serial and Parallel Execution .....	35
<i>J. Swensen and Y. Patt</i>	
 <b>Special Purpose Hardware</b>	
Performance Analysis and Design of a Logic Simulation Machine .....	46
<i>K. Wong and M.A. Franklin</i>	
A Modular Systolic Architecture for Image Convolutions .....	56
<i>K. Doshi and P. Varman</i>	
A Template Matching Algorithm-Using Optically-Connected 3-D VLSI Architecture .....	64
<i>S. Fujita, R. Aibara, M. Yamashita, and T. Ae</i>	
 <b>Data Flow</b>	
Mapping Data Flow Programs on a VLSI Array of Processors .....	72
<i>B. Mendelson and G.M. Silberman</i>	
Analytical Modeling and Architectural Modifications of a Dataflow Computer .....	81
<i>D. Ghosal and L.N. Bhuyan</i>	
A Unified Resource Management and Execution Control Mechanism for Data Flow Machines .....	90
<i>M. Takesue</i>	
 <b>Prolog</b>	
High Performance Integrated Prolog Processor IPP .....	100
<i>S. Abe, T. Bando, S. Yamaguchi, K. Kurosawa, and K. Kiriyama</i>	
Performance Studies of a Parallel Prolog Architecture .....	108
<i>B.S. Fagin and A.M. Despain</i>	
An Experimental VLSI Prolog Interpreter: Preliminary Measurements and Results .....	117
<i>P.L. Civera, F. Maddaleno, G.L. Piccinini, and M. Zamboni</i>	

## Symbolic Architectures

Deterministic and Stochastic Modeling of Parallel Garbage Collection: Towards Real-Time Criteria .....	128
<i>O. Ridoux</i>	
The Sharing of Environment in AND-OR-Parallel Execution of Logic Programs .....	137
<i>C. Sun and Y. Tsu</i>	
Architectural Issues in Designing Symbolic Processors in Optics .....	145
<i>A. Guha, R. Ramnarayan, and M. Derstine</i>	

## Interconnection Networks

Rearrangeability of Multistage Shuffle/Exchange Networks .....	154
<i>A. Varma, and C.S. Raghavendra</i>	
Optimized Mesh-Connected Networks for SIMD and MIMD Architectures .....	163
<i>R. Beivide, E. Herrada, J.L. Balcazar, and J. Labarta</i>	
Performance Evaluation of Reduced Bandwidth Multistage Interconnection Networks .....	171
<i>D.T. Harper III and J.R. Jump</i>	

## Interprocessor Communications and Synchronization

Hardware Support for Interprocess Communication .....	178
<i>U. Ramachandran, M. Solomon, and M. Vernon</i>	
Architecture of a Message-Driven Processor .....	189
<i>W.J. Dally, L. Chao, A. Chien, S. Hassoun, W. Horwat, J. Kaplan, P. Song, B. Totty, and S. Wills</i>	
Effect of Storage Allocation/Reclamation Methods on Parallelism and Storage Requirements .....	197
<i>M. Kumar</i>	

## Memory Systems

Cache Design of a Sub-Micron CMOS System/370 .....	208
<i>J.H. Chang, H. Chao, and K. So</i>	
An Architectural Perspective on a Memory Access Controller .....	214
<i>M. Freeman</i>	
Organization and Analysis of a Gracefully-Degrading Interleaved Memory System .....	224
<i>K. Cheung, G. Sohi, K. Saluja, and D. Pradhan</i>	

## Cache Design

Correct Memory Operation of Cache-Based Multiprocessors .....	234
<i>C. Scheurich and M. Dubois</i>	
Hierarchical Cache/Bus Architecture for Shared Memory Multiprocessors .....	244
<i>A.W. Wilson, Jr.</i>	
Multiprocessor Cache Design Considerations .....	253
<i>R.L. Lee, P.-C. Yew, and D.H. Lawrie</i>	

## Register-Memory Hierarchy

Performance Evaluation of Multiple Register Sets .....	264
<i>R.J. Eickemeyer and J.H. Patel</i>	
A Performance Analysis of Automatically Managed Top of Stack Buffers .....	272
<i>T.J. Stanley and R.G. Wedig</i>	
Concepts of the System/370 Vector Architecture .....	282
<i>B. Moore, A. Padegs, R. Smith, and W. Buchholz</i>	

## Processor Architectures

WISQ: A Restartable Architecture Using Queues .....	290
<i>A.R. Pleszkun, J.R. Goodman, W.-C. Hsu, R.T. Joersz, G. Bier, P. Woest, and P.B. Schechter</i>	
Architectural Tradeoffs in the Design of MIPS-X .....	300
<i>P. Chow and M. Horowitz</i>	
The Hardware Architecture of the CRISP Microprocessor .....	309
<i>D.R. Ditzel, H.R. McLellan, and A.D. Berenbaum</i>	

<b>Author Index</b> .....	321
---------------------------	-----