

Proceedings

The 17th Annual International Symposium on COMPUTER ARCHITECTURE

May 28-31, 1990

Seattle, Washington

Technische Hochschule Darmstadt FACHBEREICH INFORMATIK BIBLIOTHEK Inventar-Nr.: <u>P052090</u> Sachgebiete: Standort:



IEEE Computer Society Press
Los Alamitos, California

Washington ● Brussels ● Tokyo

Table of Contents

General Co-Chairs' Message	v
Program Chair's Message	vii
Organizing Committee	ix
ISCA90 List of Referees	xi

Session 1A: Multiprocessor Synchronization and Sequential Consistency

Weak Ordering-A New Definition	2
<i>S.V. Adve and M.D. Hill</i>	
Memory Consistency and Event Ordering in Scalable Shared-Memory Multiprocessors	15
<i>K. Gharachorloo, D. Lenoski, J. Laudon, P. Gibbons, A. Gupta, and J.L. Hennessy</i>	
Synchronization with Multiprocessor Caches	27
<i>J. Lee and U. Ramachandran</i>	

Session 1B: Multiprocessor Network Issues

Dynamic Processor Allocation in Hypercube Computers	40
<i>P.-J. Chuang and N.-F. Tzeng</i>	
A New Approach to Fast Control of $r^2 \times r^2$ 3-Stage Benes Networks of $r \times r$ Crossbar Switches	50
<i>A. Youssef and B. Arden</i>	
Virtual-Channel Flow Control	60
<i>W.J. Dally</i>	

Session 2A: Special-Purpose Architectures

Supporting Systolic and Memory Communication in iWarp	70
<i>S. Borkar, R. Cohn, G. Cox, T. Gross, H.T. Kung, M. Lam, M. Levine, B. Moore, W. Moore, C. Peterson, J. Susman, J. Sutton, J. Urbanski, and J. Webb</i>	
Monsoon: An Explicit Token-Store Architecture	82
<i>G.M. Papadopoulos and D.E. Culler</i>	
The K2 Parallel Processor: Architecture and Hardware Implementation	92
<i>M. Annaratone, M. Fillo, K. Nakabayashi, and M. Viredaz</i>	

Session 2B: Shared-Memory Multiprocessors

APRIL: A Processor Architecture for Multiprocessing	104
<i>A. Agarwal, B.-H. Lim, D. Kranz, and J. Kubiawicz</i>	
PLUS: A Distributed Shared-Memory System	115
<i>R. Bisiani and M. Ravishankar</i>	
Adaptive Software Cache Management for Distributed Shared Memory Architectures	125
<i>J.K. Bennett, J.B. Carter, and W. Zwaenepoel</i>	

Panel Session I

Big Science Versus Little Science -- Do You Have to Build It?	136
<i>D.R. Ditzel, J.L. Hennessy, B. Rudin, A.J. Smith, S.L. Squires, Z. Zalcstein, and M.D. Hill</i>	

Session 3A: Cache Memory

An Empirical Evaluation of Two Memory-Efficient Directory Methods	138
<i>B.W. O'Krafka and A.R. Newton</i>	
The Directory-Based Cache Coherence Protocol for the DASH Multiprocessor	148
<i>D. Lenoski, J. Laudon, K. Gharachorloo, A. Gupta, and J. Hennessy</i>	
The Performance Impact of Block Sizes and Fetch Strategies	160
<i>S. Przybylski</i>	

Session 3B: Instruction Sets

Performance Comparison of Load/Store and Symmetric Instruction Set Architectures	172
<i>D. Alpert, A. Averbuch, and O. Danieli</i>	
Reducing the Cost of Branches by Using Registers	182
<i>J.W. Davidson and D.B. Whalley</i>	
An Investigation of Static Versus Dynamic Scheduling	192
<i>C.E. Love and H.F. Jordan</i>	

Session 4A: Processor Implementations

VAX Vector Architecture	204
<i>D. Bhandarkar and R. Brunner</i>	
Multiple Instruction Issue in the NonStop Cyclone Processor	216
<i>R.W. Horst, R.L. Harris, and R.L. Jardine</i>	

Session 4B: Applications

Performance of an OLTP Application on Symmetry Multiprocessor System	228
<i>S.S. Thakkar and M. Sweiger</i>	
The Impact of Synchronization and Granularity of Parallel Systems	239
<i>D.-K. Chen, H.-M. Su, and P.-C. Yew</i>	

Session 5A: Memory Traces and Simulation

Trace-Driven Simulations for a Two-Level Cache Design in Open Bus Systems	250
<i>H.O. Bugge, E.H. Kristiansen, and B.O. Bakka</i>	
Performance Measurement and Trace Driven Simulation of Parallel CAD and Numeric Applications on a Hypercube Multicomputer	260
<i>J.-M. Hsu and P. Banerjee</i>	
Generation and Analysis of Very Long Address Traces	270
<i>A. Borg, R.E. Kessler, and D.W. Wall</i>	

Session 5B: Prolog/Potpourri

Fast Prolog with an Extended General Purpose Architecture	282
<i>B.K. Holmer, B. Sano, M. Carlton, P. Van Roy, R. Haygood, W.R. Bush, A.M. Despain, J.M. Pendleton, and T. Dobry</i>	
Architectural Support for the Management of Tightly-Coupled Fine-Grain Goals in Flat Concurrent Prolog	292
<i>L. Alkalaj, T. Lang, and M. Ercegovac</i>	
Balance in Architectural Design	302
<i>S. Ho and L. Snyder</i>	

Session 6A: I/O

A Study of I/O Behavior of Perfect Benchmarks on a Multiprocessor 312
A.L. Narasimha Reddy and P. Banerjee
Maximizing Performance in a Striped Disk Array 322
P.M. Chen and D.A. Patterson
A Distributed I/O Architecture for HARTS 332
K.G. Shin and G. Dykema

Session 6B: High-End Design

Boosting Beyond Static Scheduling in a Superscalar Processor 344
M.D. Smith, M.S. Lam, and M.A. Horowitz
The TLB Slice--A Low-Cost High-Speed Address Translation Mechanism 355
G. Taylor, P. Davies, and M. Farmwald
Improving Direct-Mapped Cache Performance by the Addition of a Small Fully-Associative
Cache and Prefetch Buffers 364
N.P. Jouppi

Panel Session II

Better Than One Operation Per Clock: Vectors, VLIW, and Superscalar 376
*E.S. Davidson, G.S. Sohi, J.A. Fisher, G. Grohoski,
Y. Patt, J.E. Smith, and D.R. Stiles*

Author Index 377